REMARKS

The present application was filed on June 8, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 6, 13, and 20 are independent claims.

In the outstanding Office Action dated January 29, 2004, the Examiner: (i) rejected claims 1-20 under 35 U.S.C. §112, first paragraph; (ii) rejected claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,667 to Lee (hereinafter "Lee"); (iii) rejected claim 1 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 3,646,332 to Suzuki (hereinafter "Suzuki") in view of Lee; and (iv) rejected claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,943,251 to Jiang et al. (hereinafter "Jiang") in view of Lee.

With regard to the rejection of claims 1-20 under 35 U.S.C. §112, first paragraph, Applicant asserts that such claims are patentable for at least the reasons provided below. Regarding the expressions for the binary output signal S(n), in boolean logic, the expression provided by the Examiner in the Office Action in relation to FIG. 1, is functionally equivalent to the expressions for S(n) provided on page 3, line 5, of the specification and in claim 2. More specifically, the equivalence is proven using DeMorgan's Law, which states that ^(x + y) = ^x * ^y. Therefore, in simplifying a fully complemented quantity, the individual terms in the quantity are complemented instead of the entire quantity and the function between the individual terms is changed from a "*" to "+" or vice versa. Thus, ^[{p(n)*C(n-1)}+^{p(n)+C(n-1)}] = ^{p(n)*C(n-1)}*{p(n)+C(n-1)}. Accordingly, withdrawal of the rejection to claims 1-20 under 35 U.S.C. §112, first paragraph, is therefore respectfully requested.

With regard to the rejection of claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claim 1, from which claims 3-5 directly depend, is patentable.

Lee discloses an adder that includes a static logic block, a first dynamic inverter logic block, a dynamic logic block, and a second dynamic inverter logic block for generating a sum through a sum output node. Lee further describes a dynamic logic version of an adder gate that uses a combination of inverting clock signals and short circuit current paths to conditionally discharge a dynamic node. This solution consumes excess power through the dc current path of the pullup

device MN5 and MN71 in FIG. 5, with the pull-down trees. Lee also uses two clocks, CLK and inverted clock CLKB, to prevent a pre-discharge of the dynamic node NODE52. The outputs SUM and CARRY can be in a high-impedance floating state when CLK is low and neither the SUM or CARRY is evaluated at a HIGH signal. This creates a noise sensitivity problem.

Independent claim 1 of the present invention recites a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. FIGS. 1-3 of Lee disclose conventional adder circuits and fail to disclose an adder circuit having dynamic logic, since no clock signals are used as input. Further, FIGS. 4 and 5 of Lee both use inverted clock signal CLKB to drive one or more dynamic nodes. In FIG. 4, CLKB drives dynamic inversion gates 42 and 44, each of which comprises dynamic nodes. In FIG. 5, inverted clock signal CLKB drives dynamic node NODE52. Therefore, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection to claims 1 and 3-5 under 35 U.S.C. §102(b) is therefore respectfully requested.

With regard to the rejection of claim 1 under 35 U.S.C. §103(a) as being obvious over Suzuki in view of Lee, Applicant asserts that the claim is patentable for the reasons presented above. Additionally, Applicant asserts that Suzuki is non-analogous art since it does not disclose a binary adder circuit having dynamic logic. Therefore, the combination of Suzuki and Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection to claim 1 under 35 U.S.C. §103(a) is therefore respectfully requested.

With regard to the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being obvious over Jiang in view of Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claims 6, 13 and 20, from which claims 7-9, 11, 12, 14-16, 18 and 19 directly or indirectly depend, are patentable. Claims 6, 13 and 20 recite that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Jiang does not disclose dynamic logic. Thus, Jiang is non-analogous art. Further, as described above, Lee fails to disclose a circuit having

dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Therefore, the combination of Jiang and Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) is therefore respectfully requested.

In view of the above, Applicant believes that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §112, §102(b) and §103(a) rejections.

Respectfully submitted,

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